Amendments to the Claims

This listing of claims will replace all prior versions, and listings, of claims in the application.

Listing of Claims:

1. (currently amended) A system for storing a block of data, such block of data comprising different packets of data stored in correspondingly different sections of a memory, and for gathering selected portions of the stored packets and then transferring the selected portions of the gathered packets into a transmitted block of data having the selected portions appended contiguously one to the other, such memory storing the packets in word-based locations, the word-based locations having a common word width, W, the stored packets have a variable number of bytes, the bytes of the gathered selected portions of the stored packets being offset from initial byte positions of the stored packets, the packets having variable offsets, such system comprising:

a sampling register having W byte locations for storing W bytes read from a selected one of the word-based locations of the memory, such read bytes being bytes of a currently gathered one of the packets;

a barrel shifter for shifting the W bytes stored in the sampling register, such W bytes being shifted as a function of: (a) the offset of the currently gathered one of the packets; and (b) the offsets and numbers of bytes in all different, prior gathered packets processed since a current data transfer was initiated~~the number of bytes in a prior gathered one of the packets~~ to produce W bytes;

an accumulator register having W byte locations for storing the shifted ~~bytes~~ W bytes produced by the barrel shifter in response to a clock pulse;

a staging register having W byte locations, for storing the bytes stored in the accumulator register in response to a subsequent clock pulse; and

a multiplexer having W sections, each of the W sections being coupled to a corresponding one of the W byte locations of the accumulator register and a corresponding one of the W byte locations of the staging register, each one of the sections coupling to an output thereof the byte location of the accumulator register or the byte location of the staging register selectively in accordance with the number of bytes in the prior gathered ones of the packets and the number of bytes being gathered from the currently gathered one of the packets to provide at an output of the multiplexer bytes to be transmitted as the transmitted block of data having the selected portions appended contiguously one to the other.

2. (previously presented) A system for distributing different packets of data stored in continuous locations of a memory, such memory storing the packets in word-based locations, the word-based locations having a common word width, W, the stored packets have a variable number of bytes, the bytes of the distributed packets to be offset from initial byte positions, the offsets being variable, such system comprising:

a sampling register having W byte locations for storing W bytes read from a selected one of the word-based locations of the memory, such read bytes being bytes of a currently distributed one of the packets;

a barrel shifter for shifting the W bytes stored in the sampling register, such W bytes being shifted as a function of: (a) the offset of the currently distributed one of the packets; and (b) the offsets and numbers of bytes in all different, prior gathered packets processed since a current data transfer was initiated ~~the number of bytes in a prior distributed one of the packets~~ to produce W bytes;

an accumulator register having W byte locations for storing the shifted ~~bytes~~ W bytes produced by the barrel shifter in response to a clock pulse;

a staging register having W byte locations, for storing the bytes stored in the accumulator register in response to a subsequent clock pulse; and

a multiplexer having W sections, each of the W sections being coupled to a corresponding one of the W byte locations of the accumulator register and a

corresponding one of the W byte locations of the staging register, each one of the sections coupling to an output thereof the byte location of the accumulator register or the byte location of the staging register selectively in accordance with the number of bytes in the prior distributed ones of the packets and the number of bytes being distributed from the currently distributed one of the packets to provide at an output of the multiplexer.